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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 2 of 4

Complete if Known

Application Number	10757,836
Filing Date	January 16, 2004
First Named Inventor	Craig HANSEN
Group Art Unit	2183
Examiner Name	COLEMAN, ERIC
Attorney Docket Number	43876-161

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.

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Examiner Initials*	Cite No.†	
		MU v. SCEA
		5/1/07 Exhibits A-2, E-2, and F-2 to SCEA's Supplemental Invalidation Contentions filed 5/1/07 (<i>previously marked Outside Counsel Eyes Only, now released for submission</i>) (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505; USDC for the Eastern District of Texas, Marshall Division)
		7/11/07 SCEA's Second Amended Answer, Affirmative Defenses, and Counterclaims to MicroUnity's First Amended Complaint (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		7/11/07 P.R. 4-3 Joint Claim Construction Statement (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		7/11/07 P.R. 4-3 Joint Claim Construction Statement – MU's Supporting Evidence – Reference #2: Definitions of "execution" and "general purpose computer", The IEEE Standard Dictionary of Electrical and Electronics Terms, 6 th ed. (IEEE 1996), pp. 379, 451 and 1232 (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		7/11/07 P.R. 4-3 Joint Claim Construction Statement – MU's Supporting Evidence – Reference #3: Definition of "execution", Modern Dictionary of Electronics, 6th ed. revised and updated (Newnes/Butterworth-Heinemann 1997), p. 355 (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		7/11/07 P.R. 4-3 Joint Claim Construction Statement – MU's Supporting Evidence – Reference #5: 3/9/05 Joint Claim Construction and Proffering Statement in <i>MicroUnity Engineering Systems, Inc. v. Dell, Inc. and Intel Corporation</i> , No. 2-04-CV-120 (U.S.D.C., E.D. Texas) (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		8/24/07 MU's LRP 4-5(a) Opening Brief on Claim Construction, and Exhibits 1-14 (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		9/12/07 SCEA's Responsive Brief Regarding Claim Construction Pursuant to P.R. 4-5(b), and Exhibits 1-34 (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		9/17/07 LPR 4-5(c) Reply Brief on Claim Construction from <i>MicroUnity Systems Engineering, Inc.</i> , and Exhibits 15 and 16 (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		10/15/07 SCEA's Motion for Partial Summary Judgment of Invalidation for U.S. Patent Nos. 6,643,765 and 6,725,356, and Proposed Order, and Exhibits A-U (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)
		10/29/07 MU's Response Brief in Opposition to Sony's Motion for Partial Summary Judgment of Invalidation of U.S. Patent Nos. 6,643,765 and 6,725,356, and Proposed Order (<i>MicroUnity Systems Engineering, Inc. v. Sony Computer Entertainment America, Inc.</i> ; 2:05-cv-505, U.S.D.C., E.D. Texas, Marshall Division)

Examiner Signature	/Eric Coleman/	Dated Considered	06/04/2008
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*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this in an e-mail communication to the applicant. 1. Applicant's unique citation designation number (optional). 2. Applicant is to place a check mark here if English language translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or secure a benefit by the public which is to be (and by the USPTO to process) an application. Confidentiality is guaranteed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed applications form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22311-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22311-1450. If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

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Sheet	3	of	4
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		<p>BIT Data Sheet - Product Summary: B3110/B3120/B2110/B2120 Floating Point Chip Set, Bipolar Integrated Technology, Inc. (Dec. 1986)</p> <p>Colwell et al., "Architecture and Implementation of a VLIW Supercomputer," IEEE, 910-19 (1990)</p> <p>Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," IEEE Transactions on Computers, vol.37, no.8, 967-79 (Aug. 1988)</p> <p>Hwang et al., Computer Architecture and Parallel Processing, McGraw Hill Book Co., Singapore (1988) (7 pages)</p> <p>IEEE Standard for Scalable Coherent Interface (SCI), IEEE Std 1596-1992, © (1993)</p> <p>Kuck, "The Structure of Computers and Computation: Volume 1," John Wiley & Sons, Inc. (1978)</p> <p>Lowmeyer et al., "The Multiflow Trace Scheduling Compiler," (Oct. 30, 1992)</p> <p>"MIPS Digital Media Extension" (MDMX), rev. 1.0, C-1 to C-40</p> <p>"Multimedia Extension Unit for the X86 Architecture," Compag Computer Corp., Revision 0.8b (Jun. 20, 1995)</p> <p>"PA-RISC 2.0 Architecture and Instruction Set Reference Manual," Hewlett-Packard Co. (1995)</p> <p>"TRACE/300 Series: F Board Architecture," Multiflow Computer (Dec. 9, 1988)</p> <p>X86 64-Bit Extension Multimedia Instruction Set Architecture, Intel 64-bit Multimedia ISA Ratification Summit (Apr.-May 1992) [SCEA-1423558-655] (Previously marked Confidential – Counsel Eyes Only, but released for submission)</p>	
		<p>Office Action dated May 23, 2006 in related Patent Application No. 10/757,851</p> <p>Examiner Interview Summary dated October 10, 2006 in related Patent Application No. 10/757,851</p> <p>Amendment with attached Drawings filed November 21, 2006 in response to Office Action dated May 23, 2006 in related Patent Application No. 10/757,851</p> <p>Declaration of Korbin Van Dyke filed August 21, 2007 in support of Amendment filed on August 21, 2007 in response to Office Action dated February 21, 2007 in related Patent Application No. 10/757,851</p> <p>Notice of Allowance and Fee(s) Due dated November 16, 2007 in related Patent Application No. 10/757,851</p> <p>Supplemental Notice of Allowability dated February 12, 2008 in related Patent Application No. 10/757,851</p>	

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